

IN THE SPECIFICATION

Following is a marked-up version of each amended paragraph of the subject patent application. The Examiner is requested to delete the indicated paragraph and replace it with the amended paragraph. The location for each of the deleted and replaced paragraphs is also indicated.

The text immediately above the heading “FIELD OF THE INVENTION” on line 4 of page 1, as inserted by the Preliminary Amendment of October 14, 2003, should be replaced with the following:

This application claims the benefit of Application No. 09/961,477 filed on September 21, 2001, patent number 6,686,604.

The paragraph beginning on page 13, line 12, and ending on page 13, line 30 should be replaced with the following.

According to a preferred embodiment, vertical replacement gate CMOS transistors with different operating voltages are formed according to the following steps. As shown in Figure 14, first, equal-thickness initial gate oxide layers 220A, 222A, 220B and 222B are grown in the channel regions 160A, 162A, 160B and 162B, respectively, of each vertical replacement gate transistor 210A, 212A, 210B and 212B. Assuming the MOSFETs 210A and 212A are intended to operate at higher operating voltages (and therefore require a thicker gate oxide layer), they are masked according to known lithography techniques. The initial oxide layers 220B and 222B are then removed from the non-masked MOSFETs 210B and 212B. See Figure 15. The mask is removed and a second gate oxide deposition is performed. During this second gate oxidation the masked gate oxide regions 220A and 222A will grow thicker, although at a slower rate than the growth of a new oxide layers 220B and 222B on the non-masked MOSFETs 210B and 212B. See Figure 16. Thus at the conclusion of the second gate oxide deposition process, two different gate oxide thicknesses have been formed. Relatively thick gate oxides 220A and 222A have been formed for the

MOSFETs 210A and 212A, and relatively thin gate oxides 220B and 222B have been formed for the MOSFETs 210B and 212B. This process can be repeated any number of times to create any number of gate oxide thicknesses and can be applied to any number of MOSFETs on the integrated circuit.

The paragraph beginning on page 14, line 26, and ending on page 15, line 2 should be replaced with the following.

As shown in Figure 17, next the polysilicon gate regions 230 and 234 are deposited. The gate 230 pertains to the MOSFETs 210A and 212A for controlling conduction through the channels 160A and 162A. The gate 240234 pertains to the MOSFETs 210B and 212B for controlling conduction through the channels 160B and 162B. The gate regions 230 and 234 are formed over, but separated from, the conductive layer 120 by the interposing insulative layers 122, 124 and 126. Portions of the silicon nitride layers 134 and 138 and the silicon dioxide layer 136 are positioned over the gate regions 230 and 234.